

AMENDMENT UNDER 37 C.F.R. § 1.116  
Application Serial No. 10/623,660  
Attorney Docket No. Q76637

**AMENDMENTS TO THE SPECIFICATION**

**Please replace the second full paragraph on page 3 with the following amended paragraph:**

A vector process is a process (Single Instruction Multiple Data stream: SIMD) for simultaneously processing a plurality of regularly arranged data. A register which stores such a plurality of regularly arranged data is referred to as a vector ~~resistor~~register, and instructions for performing the same operation on, effecting memory access to, and transferring, all the elements stored in the vector register are referred to as vector instructions.